https://dx.doi.org/10.22161/ijaers.4.11.19 *ISSN: 2349-6495(P) | 2456-1908(O)*

Design and Analysis of RCA and CLA using CMOS, GDI, TG and ECRL Technology

Kuldeep Singh Shekhawat[1], Gajendra Sujediya[2]

[1]Research Scholar, Department of ECE, Rajasthan Institute of Engineering and Technology, Jaipur, India
[2]Assistant Professor, Department of ECE, Rajasthan Institute of Engineering and Technology, Jaipur, India

Abstract*—VLSI technology has developed over the years thereby enhancing the performance of chips in terms of three basic constraints viz. delay, power and area. In today's scenario compact and small digital devices are critical concern in the field of VLSI design, which should perform fast as well as low power consumption. Optimizing the delay, area and power of an adder is a major design issues, as area and speed are usually conflicting constraints. Adders can be designed with conventional CMOS technology but for compact and low power consumption we can design circuit using adiabatic logic and with other technology GDI,ECRL, transmission Gate.*

***Keywords*—Adders, CMOS, GDI, TG, ECRL.**

I. INTRODUCTION

Full adders can be designed using multiple techniques out of which Ripple Carry Adder (RCA) and Carry Look-ahead Adder (CLA) are considered for comparison based on their power and speed. In the designing of the digital circuits speed and power is conflict to each other. A Ripple Carry Adder consumes the least power but is the slowest (propagation delay is the most) while Carry Look-ahead Adder is the fastest but requires more power.

II. BASIC ADDER BLOCKS

2.1 HALF ADDER

The circuit is created using the combination of an XOR and an AND Gate. Each gate handles a component of the output. The AND Gate takes the input and give the carry bit and the XOR gate outputs the sum bit. A and B are the inputs and SUM and CARRY are the output signals Boolean equations for a half adder is given below:

$$SUM = A \oplus B$$

$$Carry = A \bullet B$$

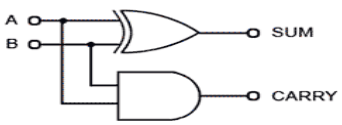

Fig.2.1. Half Adder Circuit

2.2 Full Adder

A Full adder is an extension of the half adder. This works by taking the carry bit from previous addition and using this along with the two input operand bits. This means that this adder can be used to add binary numbers with more than 1 bit. It functions by taking into account the two input bits as well as the carry bit, passing them through a set of gates and giving a sum and carry bit as the output [2]. Boolean equations for a full adder are given below:

$$S = A \oplus B \oplus C$$

$$C_{out} = A \bullet B + B \bullet C_{in} + A \bullet C_{in}$$

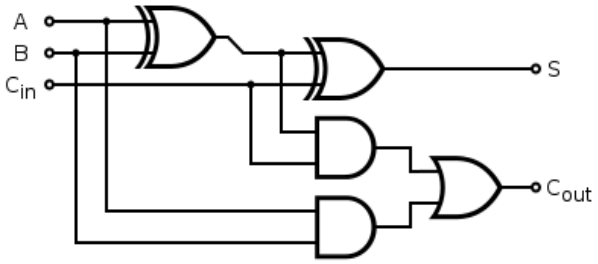

Fig.2.2. Full Adder Circuit

2.3 Multiple Bit Adders

- **Ripple-Carry Adder:** A Ripple carry adder is designed using cascading connections of multiple full adders. What this means is that the carry out signal of the preceding full adder is the carry in signal for the succeeding full adder and so on. Ripple-Carry adder is the most compact adder (O (n) Area) among all the adders. This adder can be used to design compact devices on the cost of speed as this adder is very slow (O (n) time) for computation. In case of fast addition, carry increment and carry skip architecture can be used, particularly for 8 to 16 bit lengths.
- **Carry-Look ahead Adder:** Carry-Look ahead adders (CLA) are the fastest adders, but they consume maximum area and little bit complex. This adder is preferred for addition up to 4 bit length.

III. IMPLEMENTATION

- 8-bit Ripple Carry Adders are implemented using 3 techniques – Conventional CMOS, Transmission Gate and ECRL Adiabatic.
- 8-bit Carry Look-ahead Adders are implemented

https://dx.doi.org/10.22161/ijaers.4.11.19 *ISSN: 2349-6495(P) | 2456-1908(O)*

using 4 techniques – Conventional CMOS, Transmission Gate, GDI [5] and ECRL Adiabatic.[1]

3.1 Full Adder Using CMOS technology

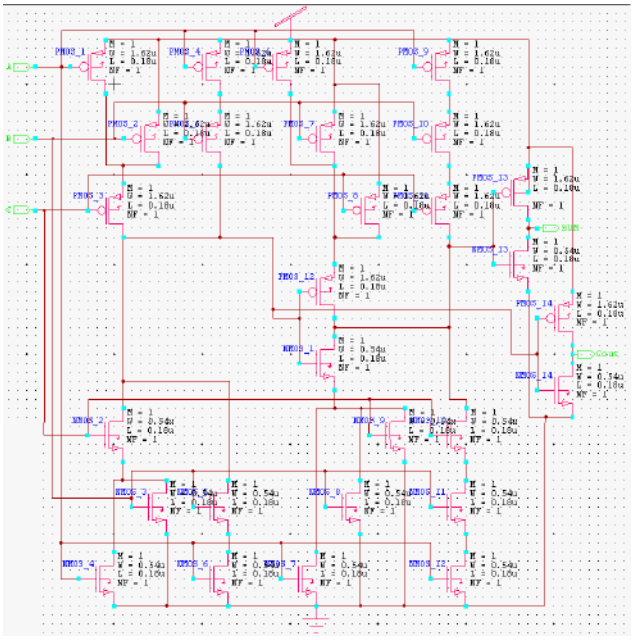

Fig.3.1. Full Adder Design Using CMOS Logic

3.2 Full Adder Using Transmission Gate Logic

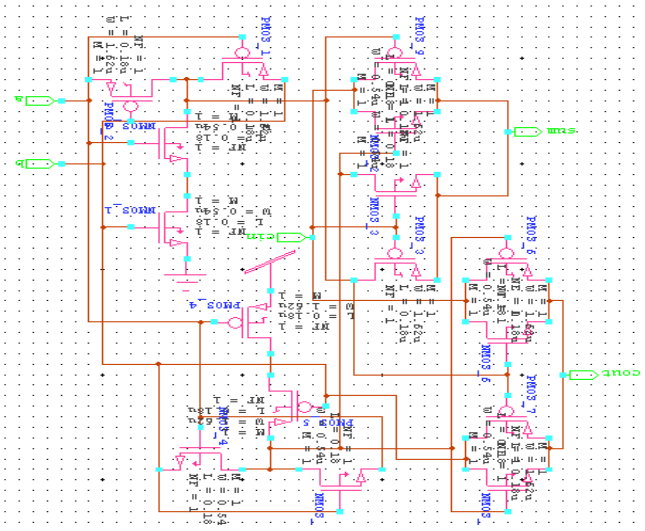

Fig.3.2. Full Adder Design Using TG Logic

3.3 Full Adder Using ECRL (Energy Charge Recovery Logic)

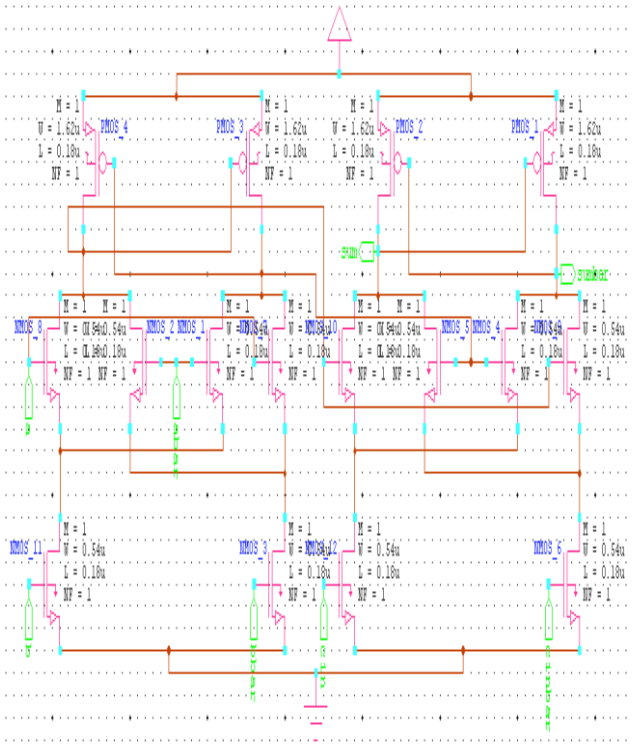

Fig.3.3.1 Sum circuit using ECRL logic

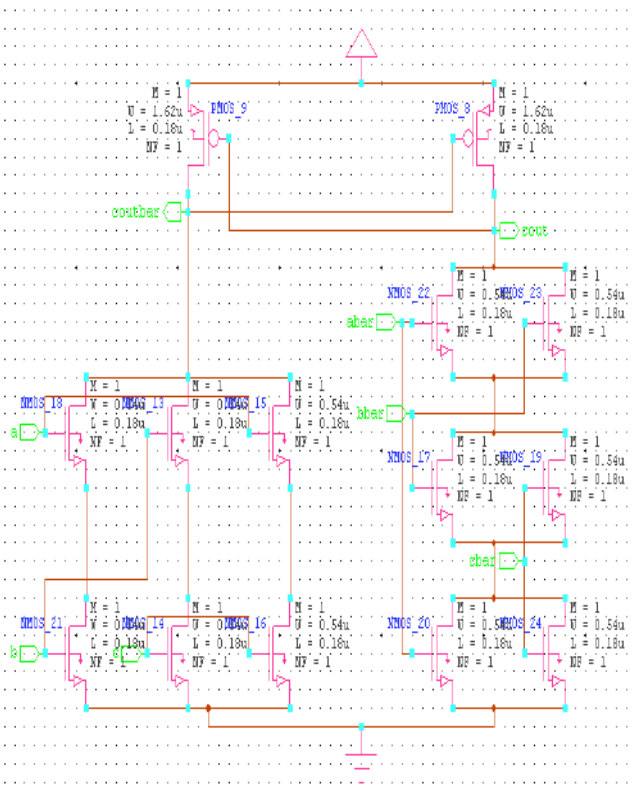

Fig.3.3.2 Carry circuit using ECRL logic

3.4 Implementation of 8-BIT RCA

For designing 8-bit adders, the corresponding 1-bit full adders described in the previous sections are used. These are cascaded together so that each carry bit from one

https://dx.doi.org/10.22161/ijaers.4.11.19 *ISSN: 2349-6495(P) | 2456-1908(O)*

adder "ripples" to the next.An RCA uses lesser number of transistors thus reducing the power dissipation.The input signals to an 8-bit adder are: a_0-a_7, b_0-b_7 and c_{in} and sum_0-sum_7 & c_{out} are the output signals.

3.4.1 Implementation of a Carry Look-Ahead Adder

CLAs utilize the concept of the generate (g), kill (k) and the propagate (p) signals.

These generate and propagate signals are represented as:

$$P_i = A_i \oplus B_i$$

$$G_i = A_i \bullet B_i$$

where, ai and bi are the input signals. The carry signal, C_{in}, and the sum signal, S_i, are given by:

$$C_{i+1} = G_i + P_i \bullet C_i$$

$$S_i = P_i \oplus C_i$$

These sum and carry signals are generated using these main components – an XOR gate, an AND gate and a $g_i+p_i.c_i$ Boolean expression logic circuit. In the following sections, working of the above mentioned components are explained for 4 different techniques – Conventional CMOS, Transmission Gate, Gate Diffusion Input and ECRL[3].

- **8-Bit CLA Using Conventional CMOS**

To design N-bit adder, N 1-bit adders are required. In the case of Carry Look-ahead adders, these 1-bit adders are designed using 2 XOR gates, 1 AND gate and a $g_i+p_i.c_i$ boolean expression logic circuit. Here, for a 1-bit adder, 19-PMOS and 19-NMOS transistors are required.

- **8-Bit CLA Using Transmission Gate (TG)**

For designing a 1-bit adder based on TG logic , the circuit components used are - 2 XOR gates and a boolean expression logic, $g_i + p_i.c_i$, circuit. The design of these circuit components is different from the way it is done in Conventional CMOS design. 1 TG based full adder has 11 PMOS and 11 NMOS transistors.

- **8-Bit CLA Using Gate Diffusion Input (GDI) Logic**

To reduce the power consumption as well as the transistor count further, another technique for creating a full adder is used, called Gate Diffusion Input (GDI). For designing a 1-bit full adder using GDI logic, only 5 PMOS and 5 NMOS transistors are required.

- **8-Bit CLA Using ECRL Adiabatic Logic**

To design a 1-bit adder using ECRL, 2 XOR gates, 1 AND gate and a ($g_i + p_i.c_i$) boolean expression logic circuit are used. It comprises of 11 NMOS and 25 PMOS transistors which is greater than that required in an RCA [4].

IV. RESULT, ANALYSIS AND COMPARISON

The design and simulations have been done using Tanner Tools 15.23.Comparison of the propagation delay and the power dissipation for different full adders is shown at varying supply voltages and operating frequencies. An RCA is designed using Conventional CMOS, TG logic and ECRL techniques and a CLA using Conventional CMOS, TG logic, GDI logic and ECRL. All the simulations are carried out at 180nm technology, NMOS transistor W/L ratio – 540/180 and PMOS transistor W/L ratio 1620/180.

4.1 Ripple Carry Adder

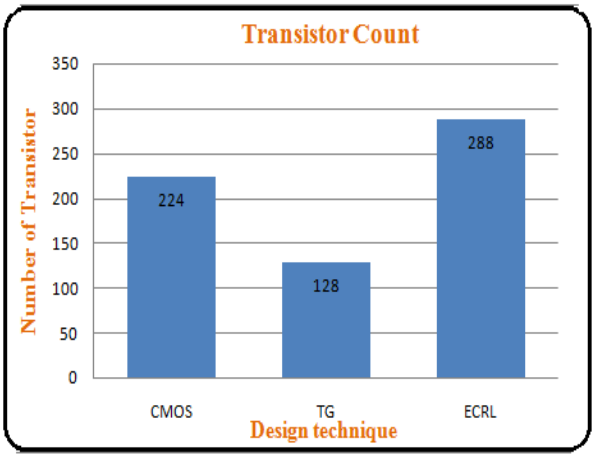

Fig.4.1.1 Transistor Count for RCA using Different Logic Design

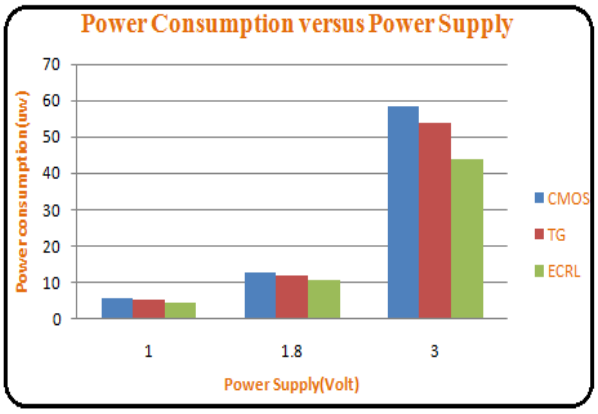

Fig.4.1.2 8-bit RCA power consumption comparison for different logic

4.2 Carry Look-ahead Adder

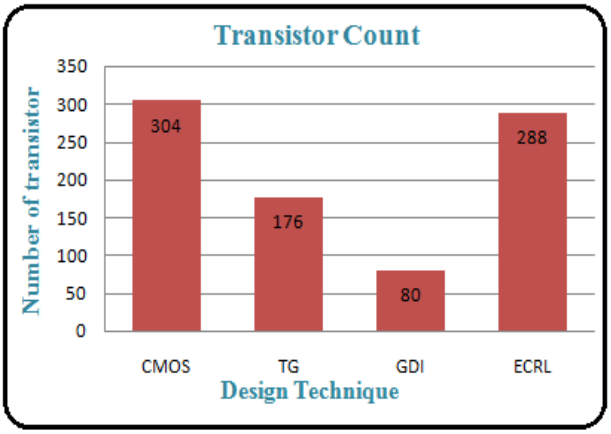

Fig.4.2.1 Transistor count for CLA using Different design technique

https://dx.doi.org/10.22161/ijaers.4.11.19 *ISSN: 2349-6495(P) | 2456-1908(O)*

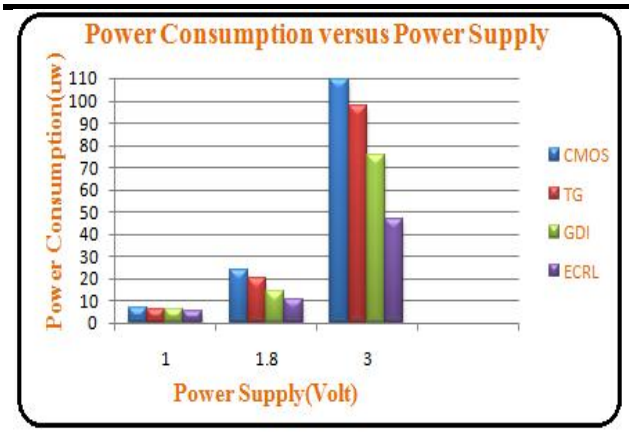

Fig.4.2.2 8 bit CLA power consumption versus power supply

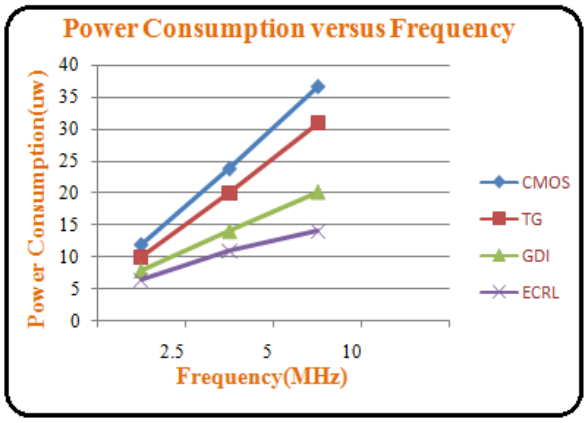

Fig.4.2.3. 8 bit CLA power consumption versus frequency

4.3 Comparative Analysis of 8-Bit RCA and CLA

By analysing 8bit RCA and CLA for different logic design for different input voltages and frequency we can see that RCA is better in terms of power consumption but delay is very high. Due to this reason, a CLA is used. To reduce the drawback of CLA power consumption we have used adiabatic logic in this work so power level decreases as in RCA circuit

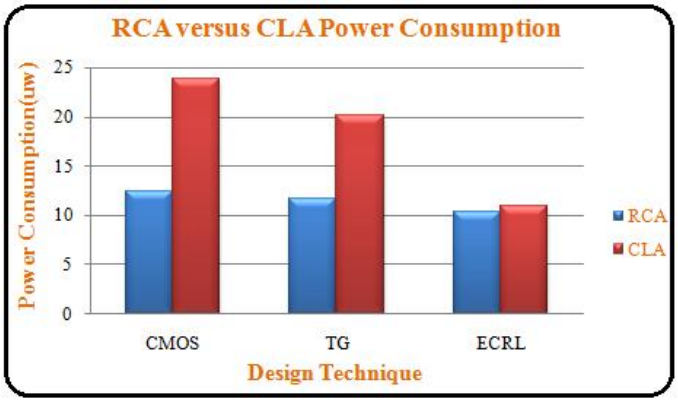

Fig.4.3.1 Power consumption for CLA and RCA

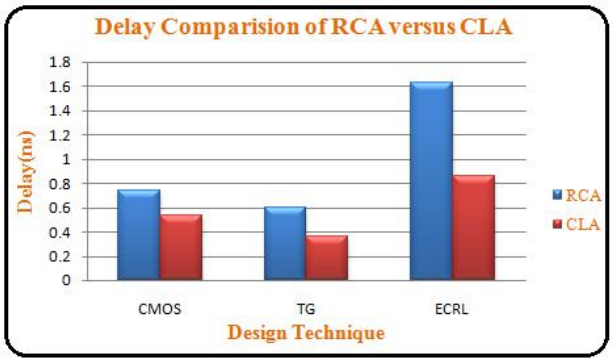

Fig.4.3.2. Delay comparison of RCA and CLA

V. CONCLUSION

When we compare Ripple Carry Adder and Carry look ahead Adder, CLA is better compare to RCA.CLA is better from RCA using ECRL adiabatic logic in which delay is reduced. And transistor count is also equal for both the logic circuits.

REFERENCES

[1] Baljinder Kaur and Narinder Sharma, "Design of Full Adder in 180nm Technology using TG and Adiabatic Logic", International Journal of Computer Techniques, vol. 3, Issue 2, pp. 164-170, Mar-Apr 2016.

[2] Kunjan D. Shinde, Jayashree C. Nidagundi, "Design of fast and efficient 1-bit full adder and its performance analysis", 2014 International Conference on Control, Instrumentation, Communication and Computational Technologies (ICCICCT), pp. 1275-1279, 2014.

[3] S.Soundarya, Ms.S.Anusooya, "Design and analysis of Low power Carry Look-ahead adder using subthreshold Adiabatic logic", International Journal of Emerging Trends in Science and Technology, vol. 3, Issue 6, pp. 891-895, June 2016.

[4] Y. Sunil Gavaskar Reddy, V.V.G.S.Rajendra Prasad, "Comparison of CMOS and Adiabatic Full Adder Circuits", International Journal of Scientific & Engineering Research, vol. 2, Issue 9, September 2011.

[5] A. Morgenshtein, A. Fish, I.A. Wagner, "Gate-diffusion input (GDI) - a technique for low power design of digital circuits: analysis and characterization", IEEE International Symposium on Circuits and Systems, vol. 1, pp. I-477 – I-480, May 2016.